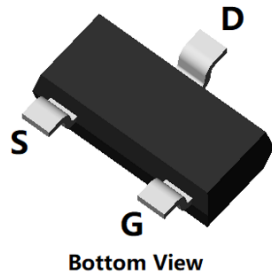
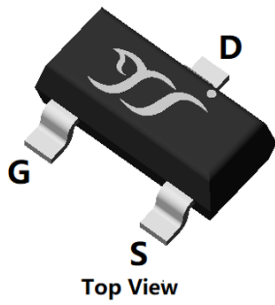
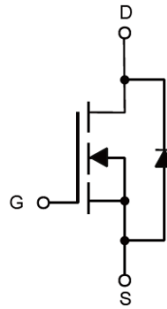


N-Channel Enhancement Mode Field Effect Transistor



SOT-23



Product Summary

• V_{DS}	30V
• I_D	5.6A
• $R_{DS(ON)}$ (at $V_{GS}=10V$)	<25mohm
• $R_{DS(ON)}$ (at $V_{GS}=4.5V$)	<31mohm
• $R_{DS(ON)}$ (at $V_{GS}=2.5V$)	<45mohm

General Description

- Trench Power LV MOSFET technology
- High density cell design for low $R_{DS(ON)}$
- High Speed switching
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Battery protection
- Load switch
- Power management

■ Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	30	V
Gate-source Voltage		V_{GS}	± 12	V
Drain Current	$T_A=25^\circ\text{C}$	I_D	5.6	A
	$T_A=70^\circ\text{C}$		4.5	
Pulsed Drain Current ^A		I_{DM}	23	A
Total Power Dissipation	$T_A=25^\circ\text{C}$	P_D	1.2	W
	$T_A=70^\circ\text{C}$		0.8	
Thermal Resistance Junction-to-Ambient ^B		$R_{\theta JA}$	104	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range		T_J, T_{STG}	-55~+150	$^\circ\text{C}$

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJL3400A	F2	3400.	3000	30000	120000	7" reel



YJL3400A

■ Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	30			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =30V, V _{GS} =0V			1	μA
Gate-Body Leakage Current	I _{GSS1}	V _{GS} =±12V, V _{DS} =0V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	0.65	0.9	1.5	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =5.6A		20	25	mΩ
		V _{GS} =4.5V, I _D =5A		23	31	
		V _{GS} =2.5V, I _D =3A		27	45	
Diode Forward Voltage	V _{SD}	I _S =5.6A, V _{GS} =0V			1.2	V
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =15V, V _{GS} =0V, f=1MHZ		630		pF
Output Capacitance	C _{oss}			55		
Reverse Transfer Capacitance	C _{rss}			71		
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V, V _{DS} =15V, I _D =5.6A		17.25		nC
Gate-Source Charge	Q _{gs}			2.1		
Gate-Drain Charge	Q _{gd}			2		
Reverse Recovery Charge	Q _{rr}	I _F =5.6A, di/dt=100A/us		1.1		ns
Reverse Recovery Time	t _{rr}			13.1		
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DS} =15V, I _D =5.6A R _{GEN} =3Ω		4.4		ns
Turn-on Rise Time	t _r			28.2		
Turn-off Delay Time	t _{D(off)}			16.2		
Turn-off fall Time	t _f			26		

A. Pulse Test: Pulse Width ≤ 300us, Duty cycle ≤ 2%.

B. R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design, while R_{θJA} is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.



YJL3400A

■ Typical Performance Characteristics

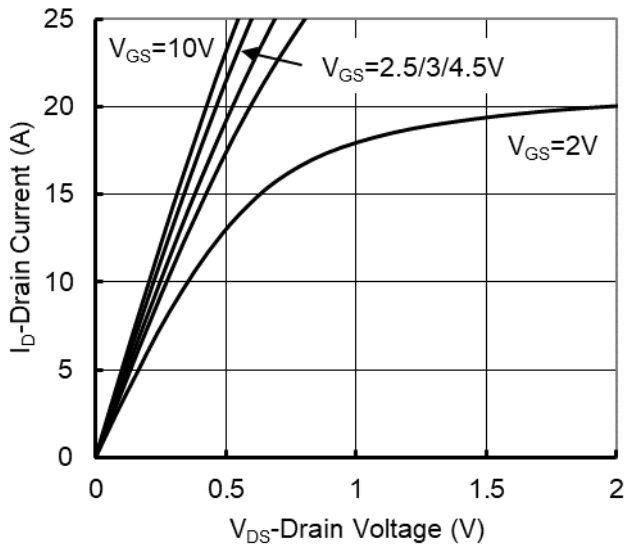


Figure1. Output Characteristics

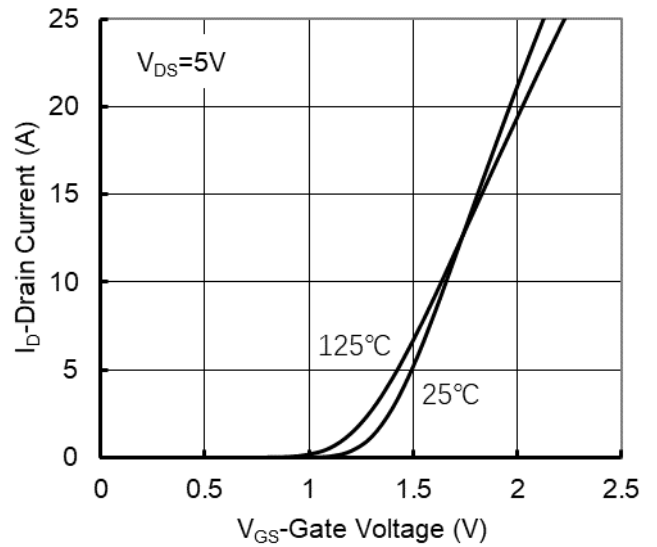


Figure2. Transfer Characteristics

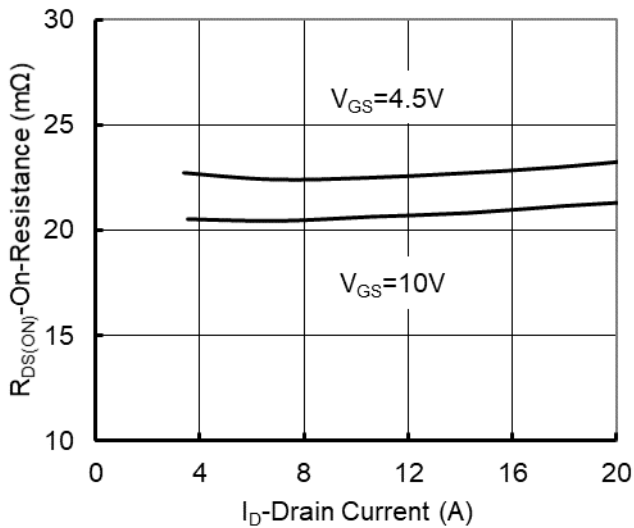


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

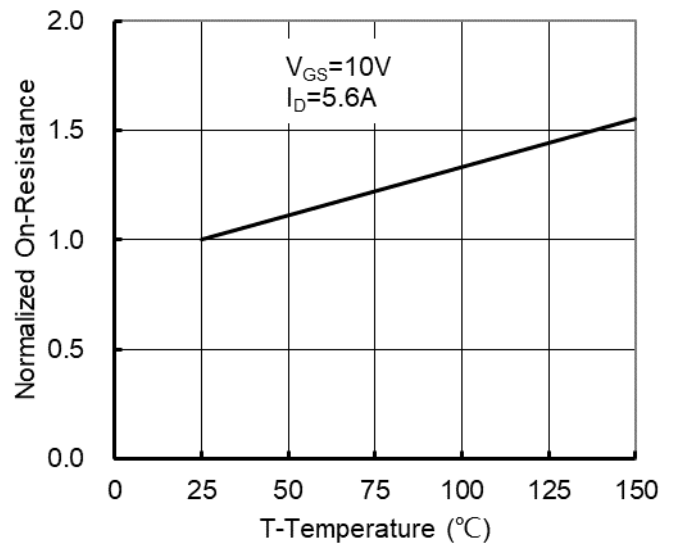


Figure 4: On-Resistance vs. Junction Temperature

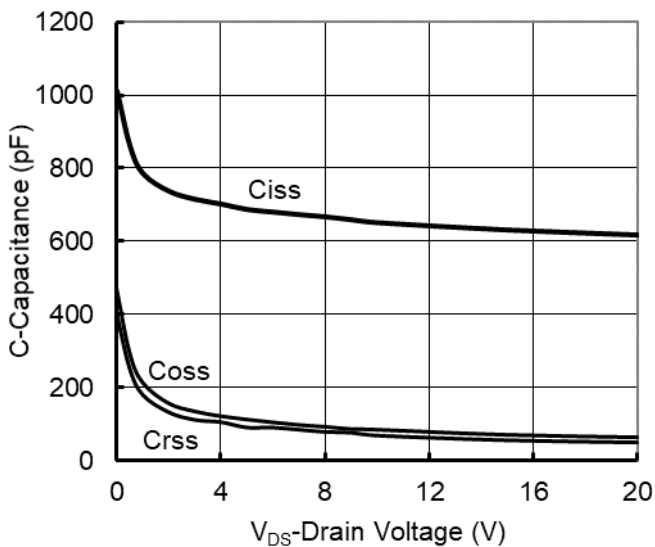


Figure5. Capacitance Characteristics

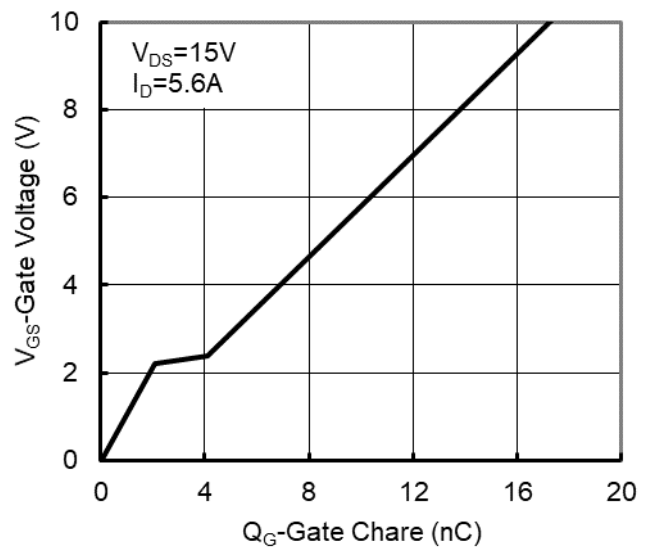


Figure6. Gate Charge



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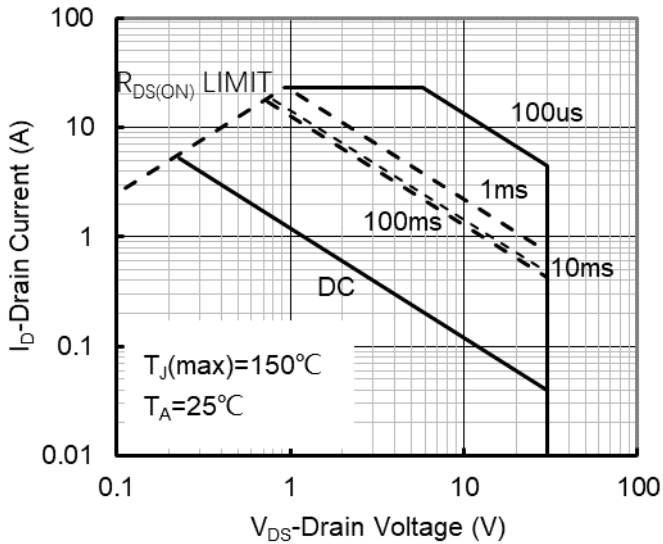


Figure7. Safe Operation Area

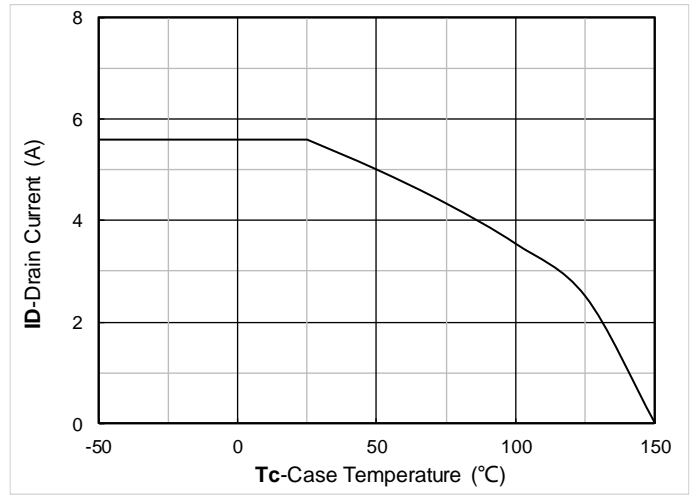


Figure8. Current dissipation

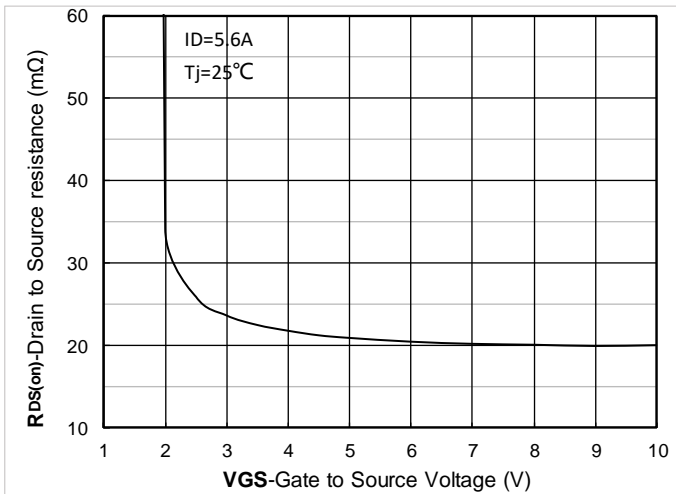


Figure 9. On-Resistance vs Gate to Source Voltage

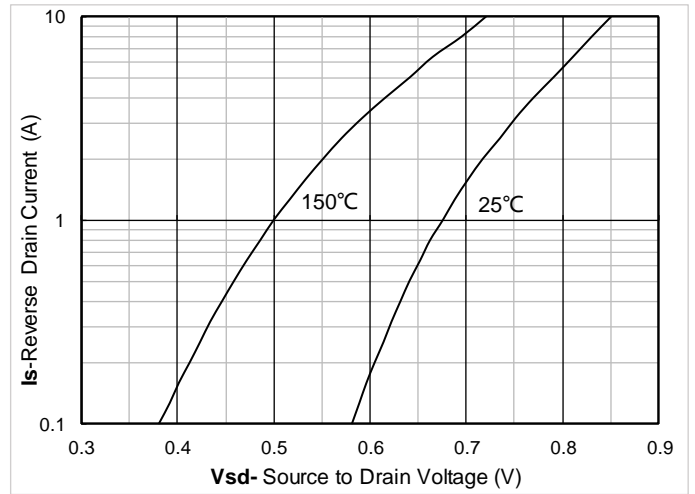


Figure 10. Forward characteristics of reverse diode

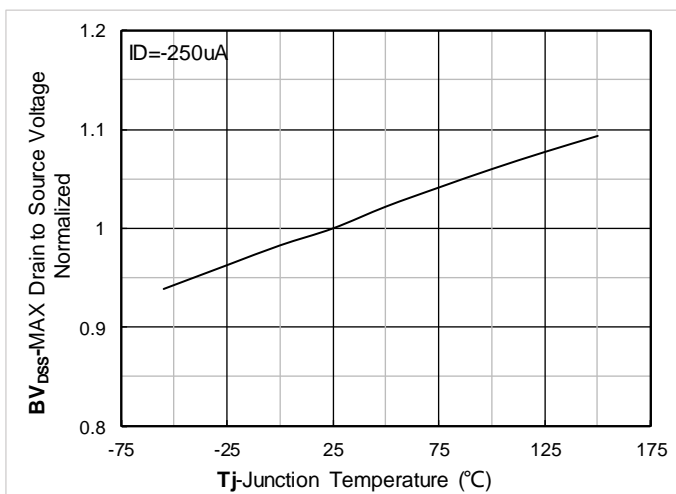


Figure 11. Normalized breakdown voltage

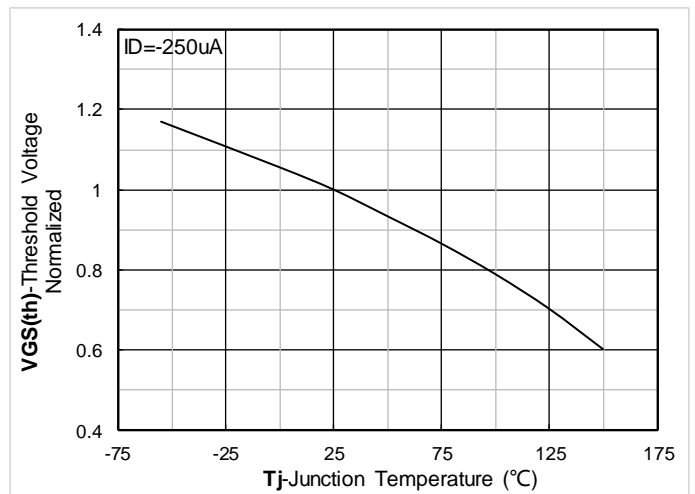


Figure 12. Normalized Threshold voltage



YJL3400A

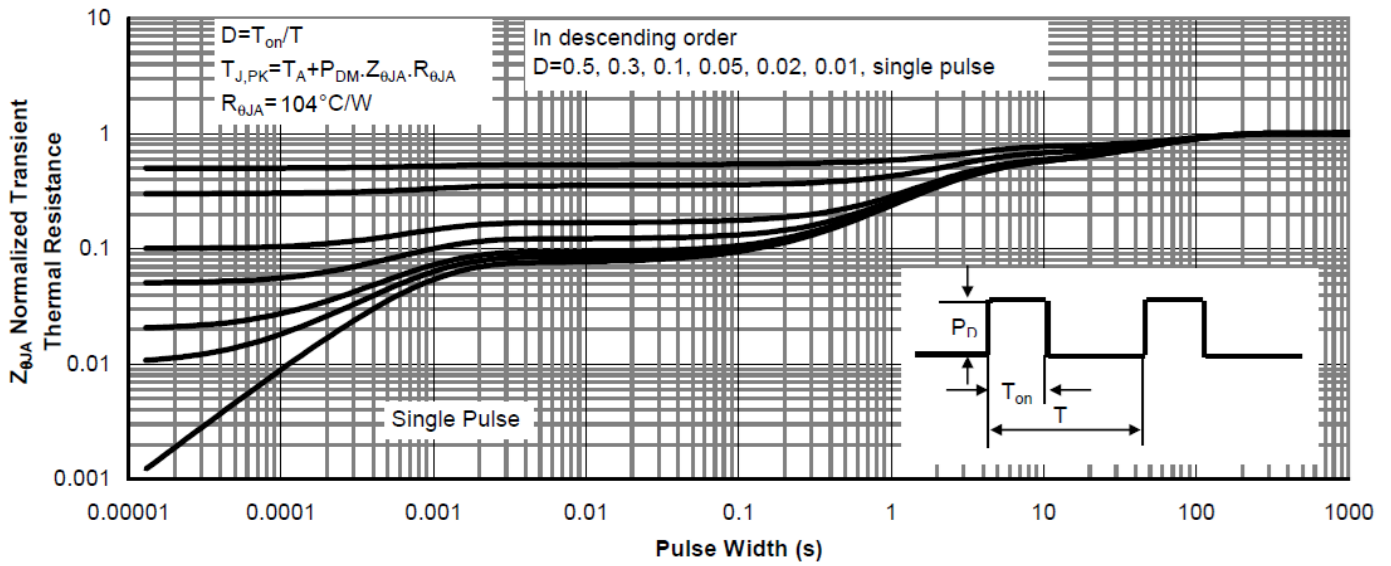
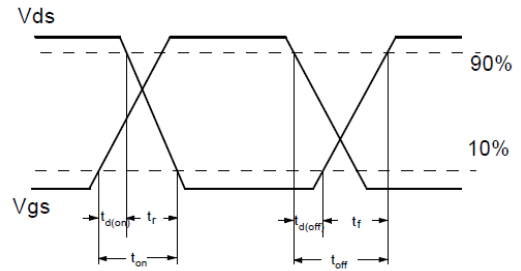
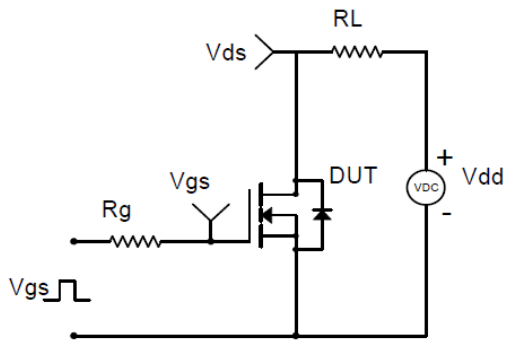
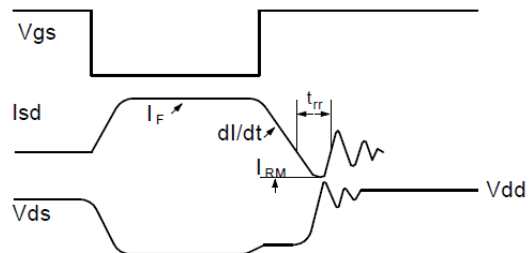
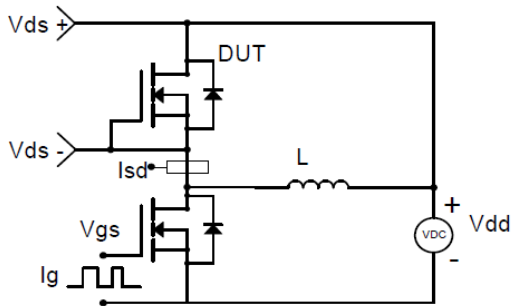


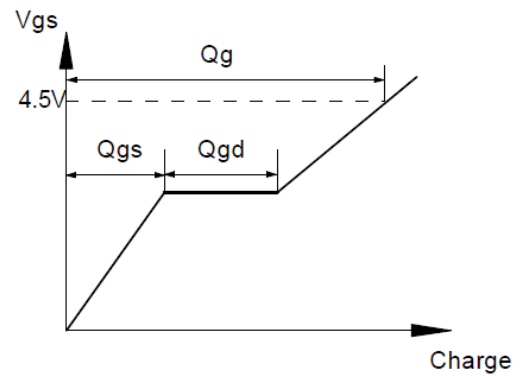
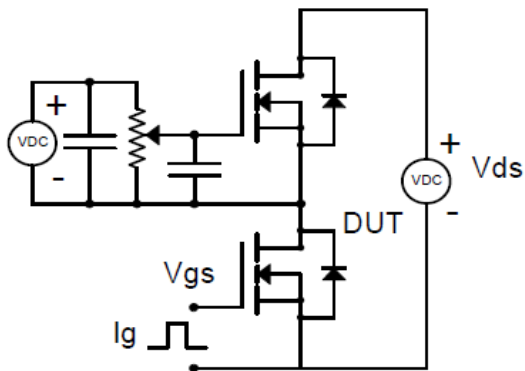
Figure13. Normalized Maximum Transient Thermal Impedance



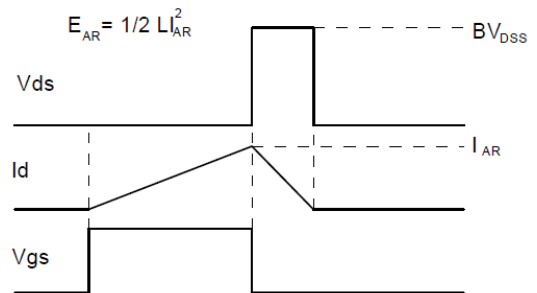
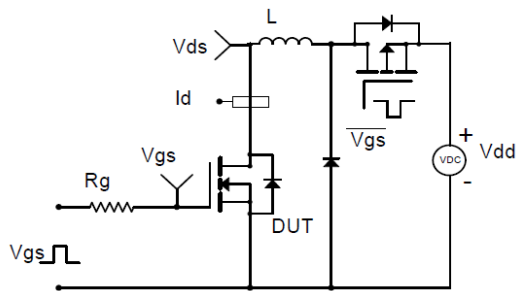
Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Gate Charge Test Circuit & Waveform

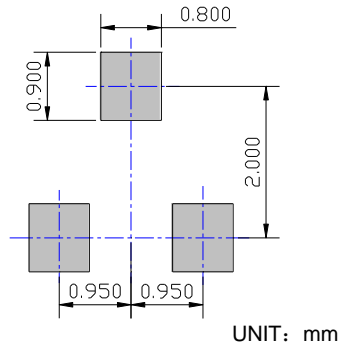
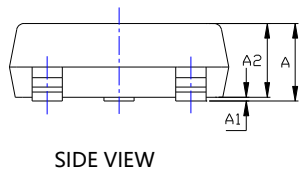
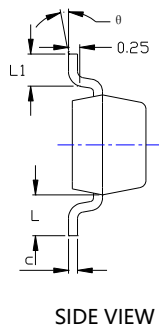
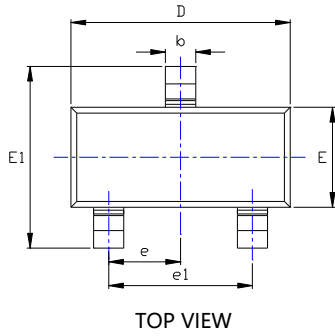


Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



YJL3400A

■ SOT-23 Package information



UNIT: mm

SYMBOL	DIMENSIONS			
	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.035	0.045	0.900	1.150
A1	0.000	0.004	0.000	0.100
A2	0.035	0.041	0.900	1.050
b	0.012	0.020	0.300	0.500
c	0.004	0.008	0.100	0.200
D	0.110	0.118	2.800	3.000
E	0.047	0.055	1.200	1.400
E1	0.089	0.100	2.250	2.550
e	0.037TYP		0.950TYP	
e1	0.071	0.079	1.800	2.000
L	0.022REF		0.550REF	
L1	0.012	0.020	0.300	0.500
θ	0°	8°	0°	8°

NOTE:

- 1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
- 2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
- 3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.



YJL3400A

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